A Frequency Hopping Microwave Radio System for Local Area Network Communications

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Abstract

This paper describes the design, development and evaluation of a frequency hopping radio transceiver operating in the 2.4-2.483GHz Industrial, Scientific and Medical (ISM) band. The principal application of the device is in portable computers where it facilitates "roving connectivity" to other portable or fixed computer systems.

1. Introduction

The introduction of portable computers has influenced the way in which computer users work. It is now possible to write a report directly into ones laptop computer during a flight and then print the document at home or back at the office. The problem is that it is necessary to make a physical connection to a printer to complete this task.

A wireless connection system has been developed which provides true "roving connectivity" for a portable computer. The system makes use of frequency hopping Spread Spectrum techniques to comply with the FCC requirements for licence free operation in the Industrial, Scientific and medical (ISM) Band. This paper describes the design of the frequency hopping radio transceiver used in this system.

2. Discussion

2a The Radio System

The requirements for the radio transceiver are summarised in the abbreviated specification shown below:

i)	Radio function	- Digitally controlled Transceiver
ii)	Operating frequency	- 83 channels 1MHz spacing 2.4-2.483GHz
iii)	Power output	- Two levels - Hi +20dBm LO +20dBm
iv)	Data input	- Serial 625 kilo Bits Sec^{-1} 5 volt logic
v)	Data output	- Serial 625 kilo Bits Sec^{-1} 5 volt logic
vi)	Receiver sensitivity	--85dBm for 10^{-5} Bit Error Rate (BER)
vii)	Channel change time	- 100μs maximum
viii)	Transmit/Receive change time	- 4μs maximum
ix)	Size	- 3" x 2" x 0.2"
x)	Power consumption	- <325mW (5v supply)

Certain parameters in the specification greatly influence the design of the transceiver. The major design "driver" is the requirement for very fast (<4μs) Transmit/Receive change over time.

This dictates the use of an up-converter/down-converter scheme where the Local Oscillator is not required to change frequency when changing from transmit to receive mode.

The radio has been developed in two stages. The first stage involved building transceivers using commercially available components, these radios have been used to prove the RF design concept and also to test the operating 'protocol'. The radio designs were then "condensed" into Application Specific Integrated Circuits (ASICS). This exercise involved reducing the IC count from forty to four!

2b Radio System Design

A schematic diagram of the basic Radio is shown in Figure 1. The design is fundamentally that of a Radio MODEM or Up/Down Converter.

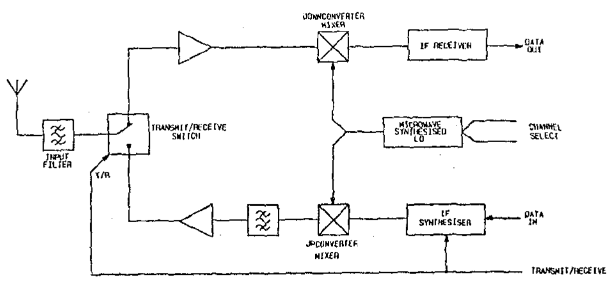

FIG. 1 UPCONVERTER/DOWNCONVERTER TRANSCEIVER SCHEME H3068543-15 ISSUE B

A Frequency Synthesised Master Oscillator (MO) feeds both an up-converter mixer (For Transmit) and a down-converter mixer (For Receive). The Master Oscillator is designed to switch frequency in a short time (<100 micro seconds) and is locked to the system reference oscillator (A Crystal Oscillator running at 10 MHz).

The Radio is designed to operate in the 2.4-2.483 GHz Industrial, Scientific & Medical Band and has a first Intermediate Frequency of 350 MHz. The MO therefore operates between 2.05 GHz and 2.133 GHz The Radio channels are spaced 1 MHz apart.

A major problem with Up/Down-Converter systems is the fact that both the Transmit and Receive IFs are at the same frequency and steps must be taken to prevent leakage of the transmit signal into the Receiver IF chain. This design employs a frequency divider in the Transmitter IF system which is disabled when the Radio is configured to receive. The transmit IF signal is generated at 700 MHz with DATA being imposed by Frequency Modulation of the Voltage Controlled Oscillator (VCO) within the 700 MHz Phase Locked Loop (PLL). (Patent filed).

A block schematic of the complete Phase Two (Non-Integrated) radio is shown in Figure 2.

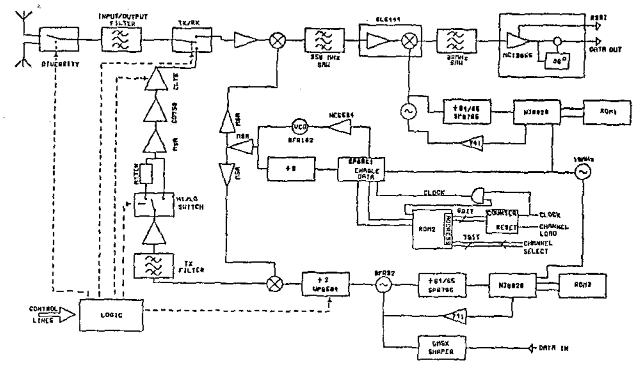

FIGURE 2 PHASE II Transceiver

2c The Receiver Section

The Receiver is a classical double conversion superhetrodyne design. Signals entering the receiver via either antenna port are fed via a Band Defining Filter to the transmit / receive switch, then to a low-noise signal amplifier. A second band-pass filter is inserted after the amplifier to suppress noise generated at the image frequency.(1.7 to 1.783 GHz) by this device. Signals are then fed to the first down-converter mixer together with Local Oscillator drive from the fast hopping synthesiser. Intermediate Frequency signals at 350 MHz are amplified and fed to a Surface Acoustic Wave Filter whose purpose is to restrict the IF band-width in order to maximise signal to noise ratio at this point. An Integrated circuit amplifier / mixer device (PLESSEY SL6444) is used to down-convert the signals to the second I F of 38 MHz, further filtering is provided by a second SAW filter. The Frequency Modulated I.F signal is de-modulated in an Integrated Circuit FM Receiver device (MOTOROLA MC 13055) This device provides a digital DATA output together with an analogue output which is used to monitor received signal strength. The LO. drive for the second down-converter at 312 MHz is generated using a Frequency Synthesiser Integrated Circuit (PLESSEY NJ 8820) which is locked to the 10 MHz system reference oscillator.

2d The Transmitter Section

Serial digital DATA is taken from the DATA input and fed to a Low Pass Filter having a Gaussian transfer response, this has the effect of limiting the bandwidth occupied by the Frequency Modulated carrier and ensures that transmissions comply with the requirements of the FCC.

The "shaped" digital signal is used to Frequency Modulate the VCO within a Phase Locked Loop operating at 700 MHz. The Frequency Modulated signal is amplified before being fed to a high speed divide-by-two circuit which is gated on and off by the Transmit/Receive control. The divider output is in the form of a 350 MHz Frequency Modulated "square-wave". It is necessary to Low-Pass filter this signal before it is amplified and fed to the Up-Converter mixer. This done to reduce the level of the harmonic energy within the signal at this point.

The Upper-Sideband output signal from the Up-Converter is selected by the use of a Band-Pass filter at the output of the mixer. This filter provides adequate suppression of the carrier and un-wanted sideband signals from the mixer. The wanted signal is of low amplitude and it is necessary to amplify at this point to a level sufficiently large to drive the output amplifier.

The output power level may be selected to be either 10 mW or 100 mW by use of the "Power Set" control, this switches an attenuator in the output amplifier causing the output level to change.

The output signal from the transmitter is fed to the Transmit/Receive switch and band defining filter before reaching the antenna selector switch and Output/Input ports.

3. The Integrated Transceiver

The radio design has been developed further to a stage where the complete transceiver may be realised using only four integrated circuits.

A block schematic of the new radio is shown in Figure 3. It can be seen that integrated design makes use of the same basic architecture as the previous design but the various radio functions have been "absorbed" into Radio Frequency Application Specific Integrated Circuits (ASICs).

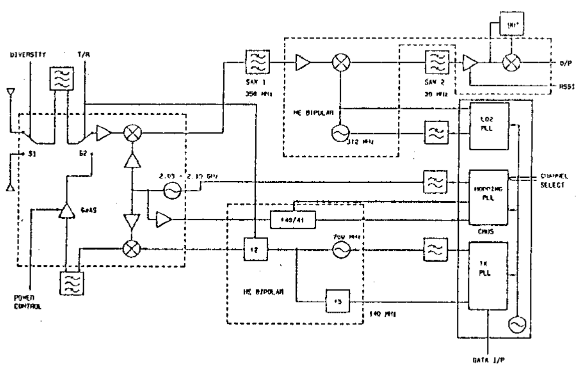

FIG 3 PHASE III TRANSCEIVER

3a The Microwave Front-End

This section of the Radio is realised as a Gallium Arsenide Microwave Monolithic Integrated Circuit.(GaAs. MiMIC) and comprises the following circuit functions:-

Antenna Selector (Diversity) Switch.
Transmit/Receive Switch.
Receiver Low Noise Amplifier.
Down-Converter Mixer.
I.F Pre-amplifier
Up-Converter Mixer.
Power Amplifier.
Microwave VCO
(for fast hopping synthesiser)

This device has been developed the design of this device with a GaAs foundry.

3b The I.F Receiver

The I.F Receiver comprises :-
The first I.F amplifier
The second down-converter
The RSSI circuitry
The second Local Oscillator
The frequency discriminator and DATA buffer

The I.F receiver is fabricated using an Advanced Silicon bipolar process and contains transistors having a transition frequency in excess of 14 GHz.

3c The Triple Synthesiser

This device is fabricated using a 1.0 micron CMOS process and comprises all the PLL components required to control the three frequency synthesisers in the radio.

3d The Oscillator/Divider

The final RF-ASIC contains the 700 MHz oscillator circuit together with the high speed, variable-modulus, pre-scaler which is used in conjunction with the microwave oscillator in the fast hopping synthesiser. This device is also fabricated using the high speed bipolar process.

4. Radio Construction

The Phase two (non-integrated) radio contains approximately 40 Integrated Circuits and 200 various passive components and is fabricated on a multi-layer Printed Circuit card having an area 7.0 inches by 5.0 inches .The new integrated radio contains only 4 integrated circuits and 50 passive components and occupies a much-reduced area of 3.0 inches by 2.0 inches. The Phase 2 and Phase 3 radios are shown in Figures 5 and 6 respectively.

5 The Radio Operating Protocol

If a number of "Wireless connectable" computers are to operate together in a network of Wireless Local Area Network (WLAN) they must all operate number the control of a Protocol. This is basically a set of rules designed to ensure that messages are passed in an orderly fashion with a minimum of "collisions" (two radios transmitting on the same frequency at the same time causing data corruption).

A scheme has been derived which makes use of "packet switching" where serial data is divided into blocks and surrounded by control data which performs both routing and validity checking functions, similar to the example shown in Figure 4.

FIELD:	FLAG	ADDRESS	CONTROL	FCS	FLAG
LENGTH:	8 BITS	112 - 560 BITS	8 BITS	16 BITS	8 BITS
CONTENTS:	01111110	CALL SIGNS & SSIDS OF DESTINATION, SOURCE, &, OPTIONALLY, DIGIPEATERS	FRAME TYPE	CALCU-LATED VALUE	01111110

FIRST BIT SENT — LAST BIT SENT

UNNUMBERED AND SUPERVISORY FRAMES

FIELD:	FLAG	ADDRESS	CONTROL	PID	INFORMATION	FCS	FLAG
LENGTH:	8 BITS	112 - 560 BITS	8 BITS	8 BITS	N x 8 BITS	16 BITS	8 BITS
CONTENTS:	01111110	CALL SIGNS & SSIDS OF DESTINATION, SOURCE, &, OPTIONALLY, DIGIPEATERS	FRAME TYPE	LAYER 3 PROTOCOL TYPE	USER DATA	CALCU-LATED VALUE	01111110

FIRST BIT SENT — LAST BIT SENT

INFORMATION FRAME

FIG 4 UNNUMBERED, SUPERVISORY AND INFORMATION FRAME FORMATS

The operating protocol must also allow the radios to operate in the presence of interference since the ISM frequency band is also the home of Microwave Ovens! This is achieved by making use of the frequency hopping capability of the radios while at the same time satisfying the requirements of FCC rule 15.247 which states that the WLAN system should use at least 75 frequencies and that the average time of occupancy on any frequency should not be greater than 0.4 seconds within a 30 second period.

6. Conclusions

A radio transceiver has been designed and produced whose performance meets the requirements of a frequency agile transmission scheme for Local Area Network applications.

The spectral properties of the radio transmitter are compliant with the requirements of the F.C.C.

The radio development has proceeded through two stages. The design and functionality was proved with a non-integraded device. The radio was then "condensed" into four Custom Asics.

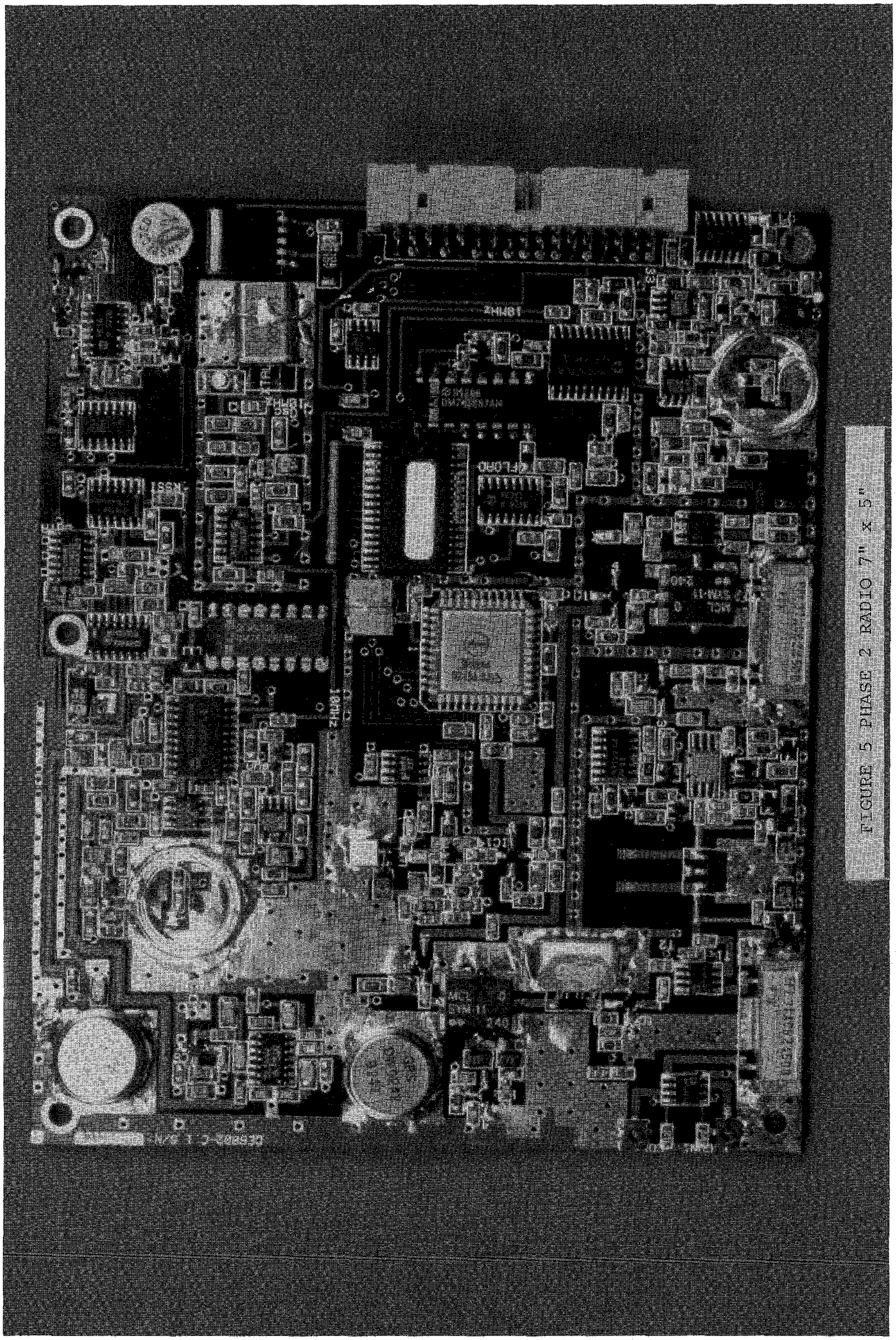

FIGURE 5 PHASE 2 RADIO 7" x 5"

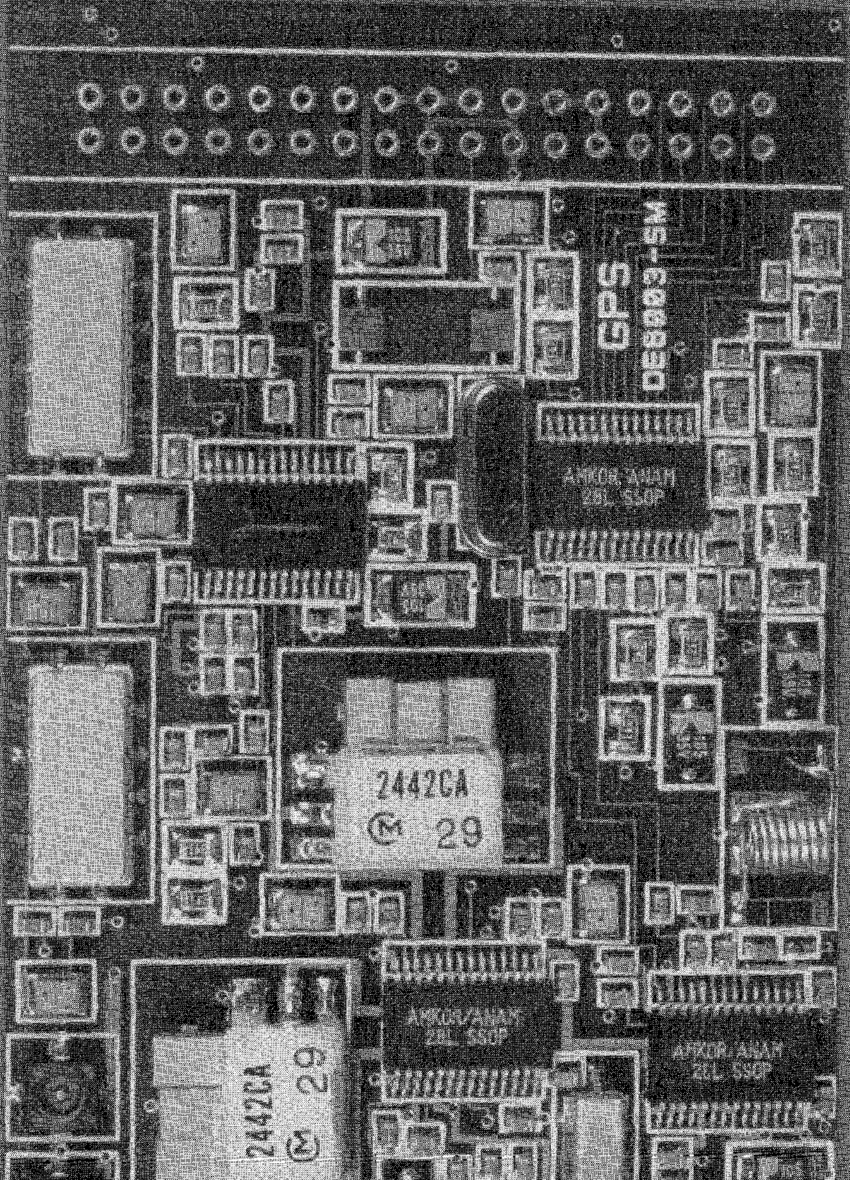

FIGURE 6 PHASE 3 RADIO 3" X 2"